

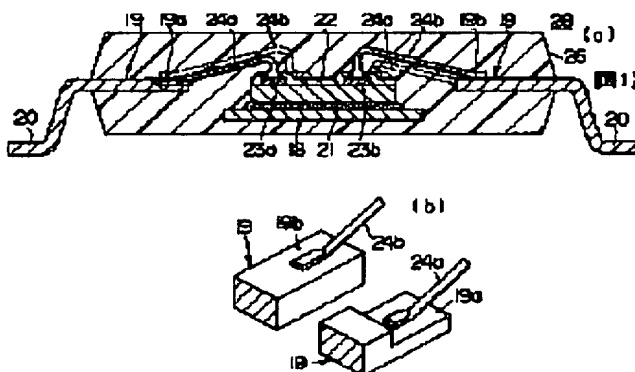
SEMICONDUCTOR DEVICE, MANUFACTURE THEREOF AND LEAD FRAME USING IT

Patent number: JP10135399
Publication date: 1998-05-22
Inventor: TANAKA SHIGEKI
Applicant: HITACHI LTD; HITACHI HOKKAI SEMICONDUCTOR
Classification:
- International: **H01L21/60; H01L23/50; H01L21/02; H01L23/48; (IPC1-7): H01L23/50; H01L21/60**
- european:
Application number: JP19960305701 19961031
Priority number(s): JP19960305701 19961031

[Report a data error here](#)

Abstract of JP10135399

PROBLEM TO BE SOLVED: To prevent mutual contact of wires in the case of a short pitch inner lead. **SOLUTION:** In a QFP(quad flat package) IC 28, pads 23 (23a, 23b) are arranged in zigzag on a pellet 22 and every other inner lead 19 is provided with a level difference 19a by half etching. A lower stage wire 24a is bonded between the outer pad 23a and the level difference 19a of the inner lead 19 whereas an upper stage wire 24b is bonded between the inner pad 23b and the level difference 19b of the inner lead 19. Upper and lower stage wires 24b, 24a are arranged contiguously while alternating. Since the gap between adjacent upper and lower stage wires 24b, 24a can be widened, wire short can be prevented even if the wire is deflected at the time of forming a resin sealing body 26. The inner lead pitch can be set wider when the wire contact margin is set equal to a conventional value.



Data supplied from the **esp@cenet** database - Worldwide